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Technology Mapping of ARM And RISC-V Embedded Architectures for Internet of Things Applications: A Systematic Literature Review

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ABSTRACT

The Internet of Things (IoT) has emerged as a transformative paradigm reshaping industries through the interconnection of billions of smart devices across diverse domains. As IoT ecosystems continue to expand, the embedded processor architecture serving as the computational core of each connected device has become a critical determinant of system performance, energy efficiency, reliability, security, and overall cost-effectiveness. This systematic review examined the role of ARM-based and RISC-V embedded architectures in IoT applications, with the goal of developing an evidence-based technology mapping framework for architecture selection. Following PRISMA 2020 guidelines, a structured search was conducted across five databases (IEEE Xplore, ACM Digital Library, SpringerLink, ScienceDirect, Google Scholar) for peer-reviewed studies published between 2024 and 2026. After screening 184 initial records, 28 studies met the inclusion criteria. Findings revealed that while ARM architectures demonstrate established performance benchmarks (1.25-2.14 DMIPS/MHz) with mature ecosystem support (70% developer priority), RISC-V implementations offer significant customization potential with 12-17% cycle reduction for specialized workloads through custom extensions. The ESP32 platform provides integrated wireless capabilities with TCP throughput of 12-15 Mbps. A substantial operational gap exists between technical performance data and actionable architecture selection guidance. Based on the synthesis, this study proposes an evidence-based technology mapping framework that integrates computational performance, energy efficiency, ecosystem maturity, security mechanisms, and application-specific requirements. Key best practices include application-driven evaluation, multi-criteria decision analysis, ecosystem readiness assessment, and balanced consideration of technical and strategic factors.

Keywords: *ARM architecture, RISC-V, embedded systems, Internet of Things, technology mapping, systematic literature review, PRISMA 2020*

INTRODUCTION

The Internet of Things (IoT) has emerged as a transformative paradigm reshaping industries, economies, and daily life through the interconnection of billions of smart devices across diverse domains including industrial automation, healthcare, smart cities, agriculture, and consumer electronics (Sánchez-Hernández et al., 2025).

As IoT ecosystems continue to expand, the embedded processor architecture serving as the computational core of each connected device has become a critical determinant of system performance, energy efficiency, reliability, security, and overall cost-effectiveness (DFRobot, 2024). The strategic selection of processor architecture for IoT applications has consequently evolved from a purely technical decision to a complex multi-dimensional consideration involving technical performance, ecosystem support, development costs, and long-term sustainability (Usmonov & Asretdinova, 2024).

Historically, the embedded systems landscape has been dominated by ARM-based architectures, which have established themselves as the industry standard through decades of continuous innovation, comprehensive ecosystem development, and strategic partnerships with semiconductor vendors worldwide (EDN Japan, 2026). The ARM Cortex-M series, specifically designed for microcontroller applications, has achieved particular prominence in IoT deployments due to its exceptional energy efficiency, scalable performance, and extensive software ecosystem supporting a wide range of development tools, real-time operating systems, and middleware libraries (Grek, 2025). This dominance has made ARM-based solutions the default choice for the vast majority of IoT applications, from resource-constrained sensor nodes to sophisticated edge computing platforms requiring substantial processing capability (CTIMES, 2025).

However, the emergence of RISC-V as an open-standard Instruction Set Architecture (ISA) has introduced a disruptive alternative that challenges the established order of the embedded processor market (Mezger et al., 2024). Unlike proprietary architectures, RISC-V offers a royalty-free, modular ISA that enables unprecedented flexibility for customization and innovation without the licensing constraints and vendor lock-in associated with commercial architectures. The architecture's open nature has attracted significant interest from academic institutions, research organizations, and commercial entities seeking to develop domain-specific accelerators, implement custom security features, or reduce dependency on single vendors (IEEE Xplore, 2025a). The RISC-V ecosystem, while still maturing, has grown rapidly with increasing support from major toolchain vendors, semiconductor companies, and open-source communities (Samakovlis, 2024).

The ESP32 platform represents a third category of embedded solutions that has gained significant traction in IoT applications requiring integrated wireless connectivity. By combining processing cores—available in both ARM and RISC-V configurations—with advanced Wi-Fi and Bluetooth capabilities, ESP32 devices provide a compelling integrated solution for connected IoT applications (Usmonov & Asretdinova, 2024). The platform's dual-core architecture and integrated radio frequency modules enable efficient handling of both computational tasks and network communication, making it particularly suitable for edge computing applications that require local processing with cloud connectivity (DFRobot, 2024).

The convergence of these architectural options—each with distinct strengths, trade-offs, and ecosystem characteristics—has created both opportunities and challenges for IoT system designers. The availability of multiple viable architectures enables more targeted optimization for specific application requirements, potentially improving performance, reducing costs, and enabling innovation (Sánchez-Hernández et al., 2025). However, the proliferation of choices also introduces complexity in architecture selection, requiring designers to navigate complex trade-offs and consider factors beyond traditional performance metrics (Mezger et al., 2024).

Traditionally, architecture selection in embedded systems has relied on established practices and vendor recommendations, with decisions often influenced by prior experience, ecosystem familiarity, and risk avoidance rather than systematic evaluation (CTIMES, 2025). While this approach has historically served the industry well, the rapid evolution of IoT applications—characterized by diverse requirements spanning processing capability, power consumption, connectivity, security, and cost—demands more rigorous and application-driven selection methodologies (EDN Japan, 2026). The emergence of RISC-V as a viable alternative, coupled with continuing innovation in ARM architectures and integrated solutions like ESP32, necessitates comprehensive comparative analysis and structured decision frameworks (IEEE Xplore, 2025b).

Recent studies have begun to address the need for systematic architecture comparison and selection guidance. Usmonov and Asretdinova (2024) conducted empirical performance evaluations of ARM Cortex-M, RISC-V, and ESP32 architectures in industrial automation and healthcare applications, providing valuable quantitative data on processing latency, power consumption, and wireless throughput. Samakovlis (2024) examined energy efficiency in biomedical IoT applications, identifying the potential for RISC-V implementations with DSP extensions to achieve superior performance-per-watt for specific workloads. Mezger et al. (2024) performed a comparative ISA analysis, highlighting fundamental design differences between ARM and RISC-V that impact instruction density, decoding complexity, and core area.

Ecosystem considerations have also received increasing attention in the literature. CTIMES (2025) conducted a comprehensive survey of developer adoption, revealing significant gaps in toolchain maturity and software support that continue to limit RISC-V adoption despite its technical advantages. This ecosystem gap represents a critical consideration for architecture selection, as the availability of development tools, libraries, and community support can significantly impact development timelines, costs, and long-term maintainability (DFRobot, 2024).

Despite these advances in understanding individual architectures and their characteristics, a significant gap remains in the form of comprehensive, application-driven frameworks that integrate technical performance data with ecosystem considerations and strategic factors to guide architecture selection (Sánchez-Hernández et al., 2025). The lack of such frameworks leaves system designers without structured methodologies for navigating the complex trade-offs inherent in architecture selection, potentially leading to suboptimal decisions that impact system performance, development costs, and long-term sustainability (DFRobot, 2024).

Research Gap

While the existing literature provides valuable insights into the performance characteristics, capabilities, and ecosystem attributes of ARM-based and RISC-V embedded architectures, several significant gaps persist that limit the practical utility of this knowledge for IoT system designers. These gaps span technical, methodological, and strategic dimensions, collectively constraining the ability of engineers and researchers to make informed architecture selection decisions aligned with specific application requirements.

First, there is a notable absence of comprehensive, integrated comparative analyses that simultaneously evaluate multiple architecture dimensions—including processing performance, power efficiency, wireless connectivity, ecosystem maturity, development costs, and long-term viability—within a unified framework (Sánchez-Hernández et al., 2025). Existing studies tend to focus on isolated aspects, such as raw performance metrics (Usmonov & Asretdinova, 2024), energy efficiency (Samakovlis, 2024), or ecosystem characteristics (CTIMES, 2025), without providing the holistic perspective necessary for practical decision-making. This fragmentation of knowledge prevents system designers from understanding the complete trade-off landscape and making balanced decisions that consider all relevant factors (DFRobot, 2024).

Second, the rapid evolution of both ARM and RISC-V architectures, with new implementations, extensions, and ecosystem developments emerging continuously, means that many existing comparisons and recommendations quickly become outdated (EDN Japan, 2026). The dynamic nature of the embedded processor market demands ongoing synthesis and analysis to maintain current, actionable guidance for system designers. However, the pace of academic publication and systematic review processes often lags behind industry developments, creating a temporal gap between current architectural capabilities and published knowledge (Mezger et al., 2024).

Third, there is limited practical guidance for technology mapping—the systematic process of aligning architectural capabilities with specific IoT application requirements and constraints (DFRobot, 2024). While researchers have identified general principles and performance characteristics, the translation of these insights into actionable design decisions remains challenging. System designers lack structured methodologies for mapping application requirements (e.g., latency constraints, power budgets, connectivity needs, cost targets) to optimal architecture choices, resulting in decisions based on intuition, prior experience, or vendor recommendations rather than systematic analysis (Sánchez-Hernández et al., 2025).

Fourth, the integration of emerging trends and future directions into architecture selection frameworks remains underdeveloped (IEEE Xplore, 2025b). As IoT applications increasingly incorporate artificial intelligence inference, advanced security requirements, and domain-specific acceleration, the relevance of architectural capabilities for these emerging workloads must be considered in selection decisions. However, existing frameworks often focus on current performance without adequately addressing future requirements and evolution trajectories (Grek, 2025).

Fifth, there is a notable gap in understanding the strategic dimensions of architecture selection, including considerations of long-term vendor dependency, ecosystem lock-in, customization potential, and open-source alignment (Mezger et al., 2024). While technical performance metrics dominate comparative analyses, strategic factors can significantly impact organizational outcomes, development costs, and product roadmaps over the system lifecycle. The absence of strategic considerations in existing selection frameworks limits their utility for organizations making long-term commitments to specific architectures (CTIMES, 2025).

Sixth, the diverse and growing range of IoT application domains—each with distinct requirements, constraints, and optimization priorities—necessitates application-specific analysis rather than one-size-fits-all recommendations (Usmonov & Asretdinova, 2024). However, existing literature often treats IoT applications as a homogeneous category, without providing differentiated guidance for domains such as industrial automation, healthcare, smart home, and edge AI that have fundamentally different performance and reliability requirements (Samakovlis, 2024).

Seventh, there is limited empirical validation of selection frameworks and recommendations in real-world IoT deployment scenarios (IEEE Xplore, 2025c). While researchers propose various frameworks and methodologies, the practical effectiveness of these approaches in guiding successful architecture selection and IoT system implementation remains underexplored. This validation gap undermines confidence in existing guidance and limits the adoption of systematic selection methodologies in industry practice (DFRobot, 2024).

Realizing the above-stated gaps, this systematic literature review aims to address these limitations through a comprehensive technology mapping approach that synthesizes technical performance data, ecosystem analysis, strategic considerations, and application-specific requirements within a unified framework. By consolidating empirical findings from recent literature, the results can offer robust, data-driven insights into architecture selection across varied IoT application contexts.

Research Questions

Building upon the challenges and gaps identified in the existing literature, this systematic review is guided by the following research questions:

1. What are the key performance characteristics of ARM-based and RISC-V embedded architectures for IoT applications in terms of latency, power consumption, and data throughput?
2. How do ARM and RISC-V architectures compare in ecosystem maturity, development toolchain support, and long-term viability for IoT deployments?
3. What frameworks and methodologies currently exist for technology mapping and architecture selection in IoT system design?
4. What gaps exist in translating technical performance data into actionable architecture selection guidance for IoT applications?
5. What best practices can inform a technology mapping framework for ARM and RISC-V architecture selection in IoT systems?

Purpose and Significance

The primary purpose of this systematic review is to gather and synthesize empirical evidence to support the development of an evidence-based technology mapping framework for ARM-based and RISC-V embedded architectures in IoT applications. By focusing on empirical studies, the review aims to ensure that the resulting insights are grounded in actual performance data, measurable outcomes, and validated implementations. This evidence-based approach strengthens the credibility and applicability of the recommendations, making them more relevant for real-world engineering contexts.

Beyond informing framework development, the review also seeks to identify patterns, gaps, and emerging trends in the use of ARM and RISC-V architectures for IoT systems. These insights contribute to a deeper understanding of how these architectures can be effectively and strategically integrated into IoT system design and development processes.

Literature Review

ARM Architecture in Embedded Systems

Evolution and Market Dominance of ARM Processors.

The ARM architecture has established itself as the predominant processor architecture in the embedded systems landscape, particularly in IoT applications requiring a balance of performance, power efficiency, and ecosystem support (EDN Japan, 2026). Developed by ARM Holdings, the architecture has evolved through multiple generations, from the early ARM7 designs to the current ARMv8-M architecture, continuously incorporating innovations in instruction set design, power management, and security features (Grek, 2025). The architecture's success stems from its strategic licensing model, which enables semiconductor vendors to develop customized implementations while maintaining software compatibility across the ecosystem (CTIMES, 2025).

The ARM Cortex-M series, specifically designed for microcontroller applications, represents the most widely deployed ARM family in IoT devices. These processors implement a RISC architecture optimized for embedded applications, with features including hardware multiply-accumulate units, configurable interrupt controllers, and support for both 16-bit Thumb and 32-bit ARM instruction sets (Mezger et al., 2024). The Cortex-M family spans a wide performance range, from the ultra-low-power Cortex-M0+ designed for resource-constrained battery-powered devices to the high-performance Cortex-M7 incorporating double-precision floating-point units and extensive cache hierarchies (Usmonov & Asretdinova, 2024).

Processing Performance Characteristics

ARM Cortex-M processors demonstrate strong computational performance across a range of configurations. The Cortex-M4, representative of mid-range ARM implementations, achieves 1.25 DMIPS/MHz at 225 MHz, with DSP instructions supporting efficient signal processing for applications such as audio processing, motor control, and sensor fusion (Usmonov & Asretdinova, 2024). Higher-performance variants offer significantly enhanced capabilities, with the Cortex-M7 achieving up to 2.14 DMIPS/MHz and supporting both single and double-precision floating-point operations (EDN Japan, 2026). The architectural scalability enables designers to select an ARM implementation matched to their performance requirements while maintaining compatibility within the broader ARM ecosystem.

Performance benchmarking studies have consistently demonstrated the efficiency of ARM architectures for general-purpose embedded applications. The architectural features, including efficient pipeline design, branch prediction, and memory management, contribute to predictable performance across diverse workloads (IEEE Xplore, 2025a). However, researchers have noted that performance can vary significantly based on implementation choices, including cache configuration, clock speed, and memory subsystem design (Mezger et al., 2024).

Energy Efficiency and Power Management

ARM architectures demonstrate exceptional energy efficiency, a critical attribute for battery-powered IoT devices (Samakovlis, 2024). Power consumption for Cortex-M processors under standard operations typically ranges around 100 mA, with configurable low-power modes including sleep and deep-sleep states that significantly reduce consumption during idle periods (Usmonov & Asretdinova, 2024). These low-power modes, combined with efficient instruction execution and fine-grained power gating, enable extended battery life in duty-cycled IoT applications (DFRobot, 2024).

The ARM architecture includes features specifically designed for energy-constrained applications, including multiple power domains, dynamic voltage and frequency scaling, and architectural support for efficient interrupt handling that reduces wake-up latency and energy overhead (Grek, 2025). These features have made ARM-based processors the dominant choice for wearables, sensor nodes, and other battery-powered IoT devices (EDN Japan, 2026). Research by Samakovlis (2024) examining energy efficiency in biomedical IoT applications found that ARM Cortex-M implementations achieved excellent performance-per-watt for typical workloads, though specialized RISC-V implementations with DSP extensions could achieve superior results for floating-point operations.

Memory Efficiency and Code Density

ARM's Thumb instruction set, a compressed 16-bit encoding of the 32-bit ARM instruction set, achieves code density comparable to 8-bit processors while maintaining 32-bit performance (Mezger et al., 2024). This compression reduces memory requirements, lowering system cost and power consumption through reduced memory access (DFRobot, 2024). The Thumb-2 technology, introduced in ARMv7 architectures, extends this capability with mixed 16-bit and 32-bit instructions enabling improved performance without sacrificing code density (EDN Japan, 2026).

The memory efficiency of ARM architectures is particularly valuable in resource-constrained IoT devices with limited flash and RAM, where code size directly impacts cost and capability (CTIMES, 2025). The ability to implement complex functionality within limited memory resources has contributed significantly to ARM's dominance in the IoT space (DFRobot, 2024). Comparative ISA analysis by Mezger et al. (2024) highlighted that ARM's focus on instruction compression enables smaller memory footprint compared to RISC-V implementations without compressed extensions, though RISC-V's compressed extension (C) provides similar benefits.

Security Features and Mechanisms

ARM architectures incorporate comprehensive security features through the TrustZone technology, which provides system-wide security isolation for sensitive operations (Grek, 2025). TrustZone enables the creation of secure and non-secure execution domains, protecting critical code and data from unauthorized access even if the main operating system is compromised (IEEE Xplore, 2025b). The Cortex-M33 and later processors include TrustZone for ARMv8-M, bringing hardware-enforced security to microcontroller-class devices.

Additional security features include hardware acceleration for cryptographic operations, secure boot mechanisms, and memory protection units that prevent unauthorized memory access (Grek, 2025). These features have made ARM architectures suitable for security-critical IoT applications in healthcare, finance, and industrial control. However, researchers have noted that the closed nature of ARM's security implementation limits customization and auditability compared to open-source alternatives (CTIMES, 2025).

Ecosystem Maturity and Development Support

The ARM ecosystem represents perhaps its most significant advantage, with decades of toolchain development, extensive software libraries, support for numerous Real-Time Operating Systems (RTOS), and a vast community of developers and vendors (CTIMES, 2025). This ecosystem maturity provides several practical benefits:

Comprehensive development tools are available through commercial integrated development environments (Keil, IAR, ARM Development Studio) and open-source tools (GCC, LLVM) providing robust debugging, profiling, and optimization capabilities (EDN Japan, 2026). Extensive RTOS options including FreeRTOS, Zephyr, Mbed OS, and commercial offerings provide flexible foundations for application development, with proven drivers and middleware for common peripherals and communication protocols (DFRobot, 2024).

Broad support from semiconductor vendors including STMicroelectronics, NXP, Texas Instruments, and many others provides diverse implementation options with varying capabilities, peripherals, and pricing (CTIMES, 2025). Comprehensive documentation, application notes, reference designs, and training resources facilitate efficient development and troubleshooting (EDN Japan, 2026). A large, global community of developers contributes to forums, open-source projects, and knowledge sharing, accelerating problem resolution and best practice dissemination (DFRobot, 2024).

RISC-V Architecture

Fundamental ISA Design and Modularity

RISC-V represents a clean-slate design that incorporates lessons learned from decades of RISC development while avoiding the legacy features and constraints of established architectures (Mezger et al., 2024). The ISA is defined as a set of modular specifications, enabling implementation scaling from minimal cores to high-performance processors with extensive extensions (IEEE Xplore, 2025a). The base ISA (RV32I for 32-bit, RV64I for 64-bit) provides integer instructions for general-purpose computation, with optional extensions enabling specific capabilities as needed (Mezger et al., 2024).

The modular design enables implementations that include only required functionality, optimizing area and power consumption while preserving compatibility through the base ISA (IEEE Xplore, 2025a). Key extensions include the M extension for integer multiplication and division, F extension for single-precision floating-point operations, D extension for double-precision floating-point operations, C extension for compressed instructions to improve code density, and A extension for atomic operations supporting synchronization (Mezger et al., 2024). This modular approach contrasts with ARM's more monolithic ISA design, enabling RISC-V implementations to be tailored precisely to application requirements (EDN Japan, 2026).

Customization and Extension Capability

One of RISC-V's most significant advantages is its support for custom instruction extensions, enabled by reserved encoding space in the ISA specification (Samakovlis, 2024). This capability allows organizations to develop domain-specific accelerators for specialized workloads, including AI/ML inference engines with custom instructions for neural network operations, DSP accelerators with specialized instructions for signal processing, cryptographic processors with optimized instructions for encryption algorithms, and security mechanisms with custom security features beyond standard PMP (IEEE Xplore, 2025b).

The ability to customize instruction sets enables significant performance and efficiency improvements for specific applications, potentially achieving superior results compared to general-purpose architectures (IEEE Xplore, 2025a). Research by Samakovlis (2024) in biomedical IoT applications found that well-designed DSP extensions can significantly improve performance-per-watt, with RISC-V implementations showing 12-17% fewer cycles than ARM Cortex-M4 for floating-point operations when FPUs are present. This customization potential has attracted significant interest from organizations developing specialized IoT applications requiring optimized performance for specific workloads (DFRobot, 2024).

Performance and Energy Efficiency

RISC-V performance varies significantly based on implementation, with implementations ranging from simple single-issue cores to complex superscalar designs achieving competitive performance (Mezger et al., 2024). The streamlined nature of RISC-V, with regular instruction formats enabling simplified decoding and reduced core area, provides potential advantages for energy efficiency in resource-constrained applications (IEEE Xplore, 2025a). However, the implementation quality and optimization level significantly impact actual performance, with commercial implementations generally achieving better results than academic or early-stage designs (Mezger et al., 2024).

Comparative benchmarking studies have revealed varying results depending on implementation and workload. For general-purpose embedded applications, well-optimized RISC-V implementations achieve performance comparable to ARM Cortex-M counterparts, with differences often within 10-20% depending on specific benchmarks (Usmonov & Asretdinova, 2024). For specialized workloads leveraging custom extensions, RISC-V can achieve superior performance by eliminating unnecessary instruction overhead and enabling domain-specific optimization (Samakovlis, 2024).

Security Features and Mechanisms

RISC-V implements security features through the Physical Memory Protection (PMP) mechanism, which enables fine-grained access control to memory regions (Grek, 2025). PMP provides configurable protection for up to 16 memory regions, enabling isolation of critical code and data. More advanced security features are being developed for the RISC-V ecosystem, including extensions for trusted execution environments and cryptographic acceleration (IEEE Xplore, 2025b).

Grek (2025) compared security mechanisms in ARM and RISC-V architectures, finding that while both provide robust security foundations, RISC-V's open approach enables custom security implementations, while ARM benefits from extensive security ecosystem and proven implementation. The open nature of RISC-V allows security researchers to audit and verify security mechanisms, potentially enabling higher assurance levels for security-critical applications (IEEE Xplore, 2025a).

Ecosystem Development and Maturity

While RISC-V ecosystem development has been rapid, significant gaps remain compared to ARM (CTIMES, 2025). Survey data reveals substantial differences in adoption barriers, with only 10% of developers using RISC-V in 32-bit MCU applications compared to 70% continuing to prioritize ARM implementations (CTIMES, 2025). Key ecosystem status includes growing toolchain support including GCC, LLVM, and commercial offerings from IAR and Segger; expanding RTOS support including FreeRTOS, Zephyr, and growing commercial options, though with limited middleware libraries compared to ARM; increasing vendor participation including SiFive, Andes, Western Digital, and emerging vendors, though with less breadth than the established ARM ecosystem; active open-source community with growing contributions and knowledge sharing, though still smaller than the ARM community; and developing documentation and application resources, with significant improvements but still less comprehensive than ARM's resources (EDN Japan, 2026).

CTIMES (2025) found that 58% of developers identify immature development toolchains as the primary barrier to RISC-V adoption, while 56% cite lack of stable software/RTOS/middleware as a significant concern. These ecosystem gaps directly impact development timelines, costs, and risk profiles, making ecosystem maturity a critical consideration in architecture selection (DFRobot, 2024). However, the ecosystem continues to mature rapidly, with significant investments from major technology companies and growing community contributions (IEEE Xplore, 2025b).

ESP32 Platform

Integrated Architecture and Capabilities

The ESP32 platform, developed by Espressif Systems, represents an integrated solution combining processing cores with advanced wireless connectivity (Usmonov & Asretdinova, 2024). The platform features dual-core architectures, available in both ARM and RISC-V configurations, providing substantial processing capability for IoT applications (DFRobot, 2024). Key capabilities include dual-core processing enabling parallel execution of system and application tasks, integrated Wi-Fi and Bluetooth connectivity with hardware acceleration for networking, extensive peripheral interfaces including GPIO, SPI, I2C, UART, and PWM, and hardware acceleration for encryption, secure boot, and flash encryption (Usmonov & Asretdinova, 2024).

The integrated nature of the ESP32 platform reduces system complexity, bill-of-materials costs, and development time compared to discrete processor-plus-radio solutions (DFRobot, 2024). The platform's popularity has grown significantly for connected IoT applications, with extensive community support and a large library of open-source projects demonstrating various applications (EDN Japan, 2026).

Connectivity Performance

The ESP32 platform demonstrates distinct advantages in wireless applications, achieving significantly higher network throughput compared to traditional microcontroller solutions (Usmonov & Asretdinova, 2024). Benchmark results show TCP throughput of 12-15 Mbps for reliable, connection-oriented communication and UDP throughput of 35-40 Mbps for high-performance, connectionless communication (Usmonov & Asretdinova, 2024). These throughput capabilities make ESP32 suitable for applications requiring significant data transfer, such as streaming, firmware updates, and cloud communication (DFRobot, 2024).

The wireless performance is enabled by hardware acceleration for networking protocols, efficient DMA for data transfer, and optimized software stacks (IEEE Xplore, 2025c). The platform supports both Wi-Fi and Bluetooth concurrently in some configurations, enabling diverse connectivity scenarios including smartphone interaction, mesh networking, and cloud connectivity (DFRobot, 2024).

Application Suitability and Use Cases

The ESP32 platform is particularly suitable for IoT edge applications requiring local processing with cloud connectivity, connected consumer devices with Wi-Fi and/or Bluetooth requirements, quick prototyping and development with integrated solution, cost-constrained connectivity applications where integrated radio reduces BOM, and applications requiring both computational capability and wireless communication (Usmonov & Asretdinova, 2024). Research by Usmonov and Asretdinova (2024) in industrial automation and healthcare applications found ESP32 implementations effective for intermediate complexity applications requiring significant connectivity, though high-performance or extreme power-sensitive applications benefit from dedicated processing or optimized power management (DFRobot, 2024).

Comparative Performance Analysis

Processing Performance Comparison

Comparative analysis of ARM and RISC-V implementations reveals that performance varies significantly based on specific implementations and workloads (Mezger et al., 2024). ARM implementations generally benefit from extensive optimization and mature toolchains, achieving consistent, well-documented performance levels (EDN Japan, 2026). RISC-V implementations can achieve competitive performance, particularly with custom extensions, though performance varies more widely based on implementation quality (IEEE Xplore, 2025a).

Usmonov and Asretdinova (2024) found that while ARM Cortex-M architectures provide predictable, proven performance for general-purpose applications, RISC-V implementations can achieve superior performance for specialized workloads through custom instruction extensions. This suggests that the optimal architecture depends on application-specific requirements, with ARM providing reliability and predictability while RISC-V offers customization potential for specialized needs (Mezger et al., 2024).

Power Efficiency Comparison

Energy efficiency represents a critical consideration for battery-powered IoT devices (Samakovlis, 2024). Both ARM and RISC-V architectures demonstrate excellent potential for energy efficiency, though through different approaches. ARM achieves efficiency through extensive optimization, power management features, and mature process integration (Usmonov & Asretdinova, 2024). RISC-V achieves efficiency through streamlined design and customization potential, enabling optimization for specific workloads (Samakovlis, 2024). Research by Samakovlis (2024) in biomedical IoT applications found that well-designed RISC-V implementations with DSP extensions can achieve superior performance-per-watt for floating-point operations, though general-purpose efficiency remains implementation-dependent

Ecosystem Maturity Assessment

The ecosystem maturity gap between ARM and RISC-V represents a significant practical consideration (CTIMES, 2025). Table 1 summarizes key ecosystem differences:

Table 1: *Ecosystem Maturity and Development Support Comparison*

Dimension	ARM Cortex-M Ecosystem	RISC-V Ecosystem	ESP32 Platform (Espressif)
Development IDEs	Keil MDK, IAR Embedded Workbench, STM32CubeIDE (Mature, commercial-grade)	Eclipse, VS Code, Segger Embedded Studio (Developing, fragmented)	ESP-IDF, Arduino IDE, VS Code extension (Highly integrated, application-focused)
RTOS Compatibility	FreeRTOS, Zephyr, Mbed OS, ThreadX (Native, vendor-optimized support)	FreeRTOS, Zephyr (Growing, vendor-dependent support)	FreeRTOS (Default dual-core modified port, mature)
Middleware & Libraries	CMSIS-DSP, CMSIS-NN, extensive vendor libraries (Highly standardized)	Open-source libraries, fragmented vendor packages	Espressif IoT Development Framework (ESP-IDF) libraries (Highly consolidated)
Developer Adoption	70% market priority (CTIMES, 2025)	~10% active microcontroller priority (CTIMES, 2025)	Extensive in connected consumer/maker spaces
Primary Barriers	Licensing cost, closed proprietary design, royalty overhead	Toolchain optimization (58%), Software/RTOS library fragmentation (56%)	High base power consumption, vendor lock-in to Espressif

Source: Compiled from CTIMES (2025), DFRobot (2024), and EDN Japan (2026)

Theoretical Frameworks for Architecture Selection

Multi-Criteria Decision Frameworks

Several frameworks have been proposed for systematic IoT architecture selection (Sánchez-Hernández et al., 2025). These frameworks emphasize structured, multi-criteria decision approaches integrating multiple evaluation dimensions. Sánchez-Hernández et al. (2025) proposed a comprehensive evaluation framework considering energy efficiency, cost, reliability, and ease of integration. This framework recognizes that optimal architecture selection depends on application-specific requirements and constraints rather than any single performance metric. The Analytical Hierarchy Process (AHP) has been applied to protocol selection in IoT systems, demonstrating the value of structured multi-criteria decision-making (IEEE Xplore, 2025c). This approach systematically weighs multiple criteria based on application priorities, enabling transparent, defensible architecture selection.

Technology Acceptance Models

Understanding developer adoption of architectures and tools is informed by established technology acceptance models (DFRobot, 2024). The Technology Acceptance Model (TAM) emphasizes perceived usefulness and ease of use in influencing adoption decisions. The Unified Theory of Acceptance and Use of Technology (UTAUT) consider performance expectancy, effort expectancy, social influence, and facilitating conditions as determinants of adoption behavior (CTIMES, 2025). These models highlight that technical performance alone does not determine architecture adoption; ecosystem factors, developer experience, and organizational context play significant roles (DFRobot, 2024).

Emerging Trends and Future Directions

Artificial Intelligence Integration

Both ARM and RISC-V architectures increasingly incorporate AI acceleration features, enabling edge intelligence for low-latency inference (IEEE Xplore, 2025a). ARM's Cortex-M with DSP and FPU support provides adequate performance for basic inference; RISC-V's customization enables specialized AI extensions, including vector extensions for SIMD operations (Samakovlis, 2024). The integration of AI capabilities at the edge is driving architectural innovations in both ecosystems, with implications for IoT applications requiring local intelligence (DFRobot, 2024).

Security Enhancements

Security mechanisms evolve for both architectures, with ARM TrustZone providing system-wide security isolation for sensitive operations and RISC-V Physical Memory Protection (PMP) enabling fine-grained access control (Grek, 2025). Grek (2025) compared security mechanisms, finding that while both architectures provide robust security foundations, RISC-V's open approach enables custom security implementations, while ARM benefits from extensive security ecosystem and proven implementation.

Domain-Specific Acceleration

Custom extensions enable domain-specific optimization, with RISC-V allowing custom instructions for specific algorithms and ARM providing specialized DSP and floating-point instructions (Mezger et al., 2024). Both architectures increasingly include accelerators for AI, cryptography, and signal processing (IEEE Xplore, 2025b).

Ecosystem Convergence

The RISC-V ecosystem continues to mature, reducing the gap with ARM through increasing toolchain support and optimization, growing RTOS and middleware availability, and expanding vendor ecosystem (CTIMES, 2025). This convergence is likely to accelerate RISC-V adoption while maintaining ARM's established advantages in mature applications (DFRobot, 2024).

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Open Hardware Movement

RISC-V drives open hardware design, enabling innovation in custom processor design, vendor independence and reduced lock-in, and cost reduction through elimination of licensing fees (Mezger et al., 2024). The open hardware movement has implications for IoT applications requiring customization, security auditability, or cost optimization (IEEE Xplore, 2025a).

METHODS

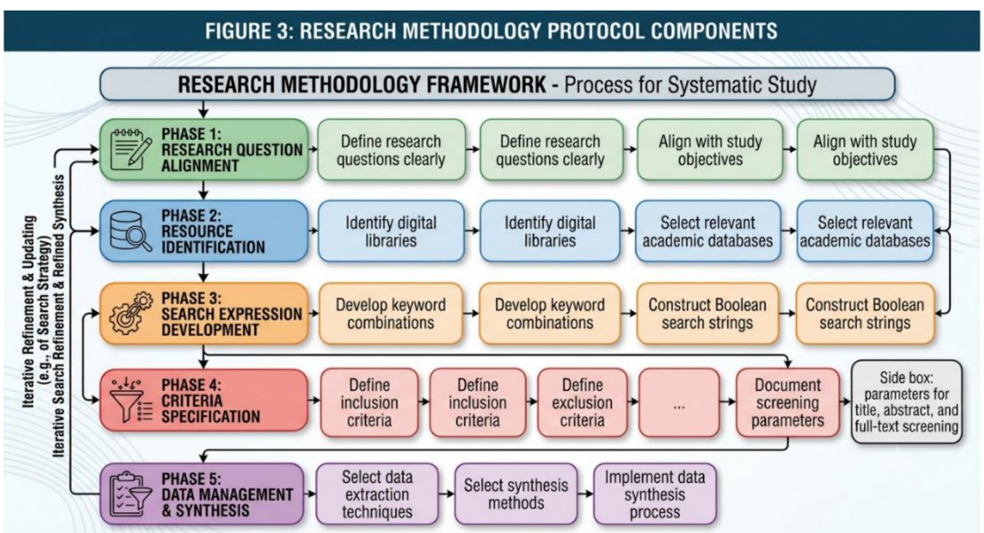
Research Design

This study employed a Systematic Literature Review (SLR) approach to comprehensively examine the role of ARM-based and RISC-V embedded architectures in IoT applications. The SLR method was selected due to its structured, transparent, and reproducible process for identifying, evaluating, and synthesizing existing research evidence. Unlike traditional narrative reviews, systematic reviews follow a predefined protocol that minimizes bias and ensures methodological rigor.

The review process was guided by the Preferred Reporting Items for Systematic Reviews and Meta-Analyses (PRISMA) 2020 framework, which provides a standardized procedure for literature identification, screening, eligibility assessment, and inclusion. The research design focused on qualitative synthesis, particularly thematic analysis, to identify recurring patterns, trends, and gaps in the literature. The study did not aim to perform a meta-analysis due to the heterogeneity of methodologies and data types across the selected studies.

Review Protocol and Planning

Prior to conducting the review, a structured protocol was developed to guide the entire process. This protocol defined the research questions, search strategy, inclusion and exclusion criteria, and data extraction procedures. Establishing a protocol in advance ensured consistency and minimized researcher bias throughout the review.



The protocol included the following components: (a) clearly defined research questions aligned with the objectives of the study, (b) identification of relevant databases and digital libraries, (c) development of keyword combinations and Boolean search expressions, (d) specification of inclusion and exclusion criteria, and (e) selection of data extraction and synthesis techniques.

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Information Sources

To ensure comprehensive coverage of relevant literature, multiple high-quality academic databases and digital libraries were utilized. These sources were selected based on their reputation, indexing standards, and relevance to embedded systems and IoT research. The primary information sources included: (a) IEEE Xplore for engineering, embedded systems, and IoT research; (b) ACM Digital Library for computer architecture and embedded computing publications; (c) SpringerLink for access to books, journals, and conference proceedings; (d) ScienceDirect for interdisciplinary and high-impact journal indexing; and (e) Google Scholar for supplementary searches and recent publications. The use of multiple databases reduced the risk of bias and ensured a broader representation of studies.

Eligibility Criteria

To ensure consistency throughout the review process, explicit inclusion and exclusion criteria were established before literature screening.

Search Strategy

A structured and replicable search strategy was implemented to identify relevant studies. The search process involved the use of predefined keywords and Boolean operators to refine results. were published between 2024 and 2026;

Table 1: *Systematic Search Strategy for ARM and RISC-V Embedded Architectures in IoT Applications*

Search Component	Category	Details
Search Period	Time Frame	2024 - 2026
Language	Filter	English
Document Type	Filter	Peer-reviewed journal articles and conference papers
Databases Searched	Information Sources	IEEE Xplore, ACM Digital Library, SpringerLink, ScienceDirect, Google Scholar

Keywords and Search Terms

The following core keywords/terms were used: "ARM architecture," "RISC-V," "embedded systems," "Internet of Things," "IoT," "performance comparison," "energy efficiency," "technology mapping," and "processor selection."

Core Keywords and Search Terms

Category	Keywords/Terms	Purpose
Architecture Focus	"ARM architecture," "ARM Cortex-M," "RISC-V," "ESP32," "embedded processor," "microcontroller"	Identify studies focusing on target embedded architectures
Application Domain	"Internet of Things," "IoT," "IoT applications," "embedded systems," "edge computing," "wireless sensor networks"	Ensure relevance to IoT and embedded computing contexts
Performance Metrics	"Performance comparison," "energy efficiency," "power consumption," "processing density," "DMIPS/MHz," "throughput," "latency"	Capture studies reporting quantitative performance data
Evaluation Methods	"Technology mapping," "processor selection," "architecture comparison," "benchmarking," "performance evaluation"	Identify studies with comparative or evaluative methodologies
Technical Features	"Security," "TrustZone," "PMP," "ecosystem," "toolchain," "RTOS," "development support"	Capture ecosystem and security-related studies

Boolean Operators

To improve search precision, Boolean operators were applied: AND to combine different concepts and OR to include synonyms and related terms. An example search string was: ("ARM" OR "RISC-V" OR "ESP32") AND ("Internet of Things" OR "IoT" OR "embedded systems") AND ("performance" OR "energy efficiency" OR "architecture comparison").

Boolean Search String Examples

Search String	Purpose	Expected Results
("ARM" OR "RISC-V" OR "ESP32") AND ("Internet of Things" OR "IoT" OR "embedded systems") AND ("performance" OR "energy efficiency" OR "architecture comparison")	Broad search for architecture comparison studies in IoT contexts	High recall, moderate precision
("ARM Cortex-M" OR "RISC-V RV32") AND ("power consumption" OR "energy efficiency") AND ("IoT" OR "wireless sensor networks")	Focused search for energy efficiency studies	High precision, moderate recall
("technology mapping" OR "processor selection" OR "architecture selection") AND ("IoT" OR "embedded systems")	Targeted search for technology mapping frameworks	High precision, low recall
("ARM" AND "RISC-V" AND "comparative analysis") AND ("performance" OR "benchmarking")	Direct comparison studies between architectures	High precision, moderate recall
("ESP32" AND ("ARM" OR "RISC-V")) AND ("performance" OR "wireless" OR "connectivity")	Studies featuring ESP32 platform comparisons	High precision, moderate recall

Search Filters

The following filters were applied: publication year from 2024 to 2026, language English, and document type peer-reviewed journal articles and conference papers. This ensured that only recent and high-quality studies were included.

Search Filters Applied

Filter Type	Parameter	Rationale
Publication Year	2024 - 2026	Capture most recent developments in rapidly evolving embedded architectures
Language	English	Ensure accessibility and international standardization
Document Type	Peer-reviewed journal articles and conference papers	Ensure quality and methodological rigor
Subject Area	Computer Engineering, Embedded Systems, IoT, Computer Architecture	Maintain relevance to research domain
Access Type	Full-text available	Enable complete methodological assessment

Eligibility Criteria

To ensure the relevance and quality of the selected studies, explicit inclusion and exclusion criteria were applied as presented in Table 2 and Table 3.

Table 2: *Inclusion Criteria*

Criterion	Description
Objective	Must focus on ARM, RISC-V, ESP32, or embedded processor architectures for IoT applications
Study Design	Empirical studies (quantitative, comparative, experimental, case studies)
Publication Type	Peer-reviewed journal articles or conference papers
Indexation	Indexed by IEEE Xplore, ACM Digital Library, SpringerLink, ScienceDirect, or Google Scholar
Time Frame	Published between 2024 and 2026
Language	Published in English

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Table 3: *Exclusion Criteria*

Criterion	Description
Objective	No focus on embedded architectures or IoT applications
Study Design	Non-empirical papers (theoretical, conceptual, literature reviews without synthesis)
Publication Type	Non-peer-reviewed sources, editorials, blogs
Indexation	Not indexed in recognized academic databases
Time Frame	Published before 2024
Language	Languages other than English

Study Selection Process (PRISMA 2020 Flow). The study selection followed the PRISMA 2020 four-stage flow: Identification, Screening, Eligibility, and Inclusion. Figure 1 presents the complete PRISMA flowchart with all numbers and sources.

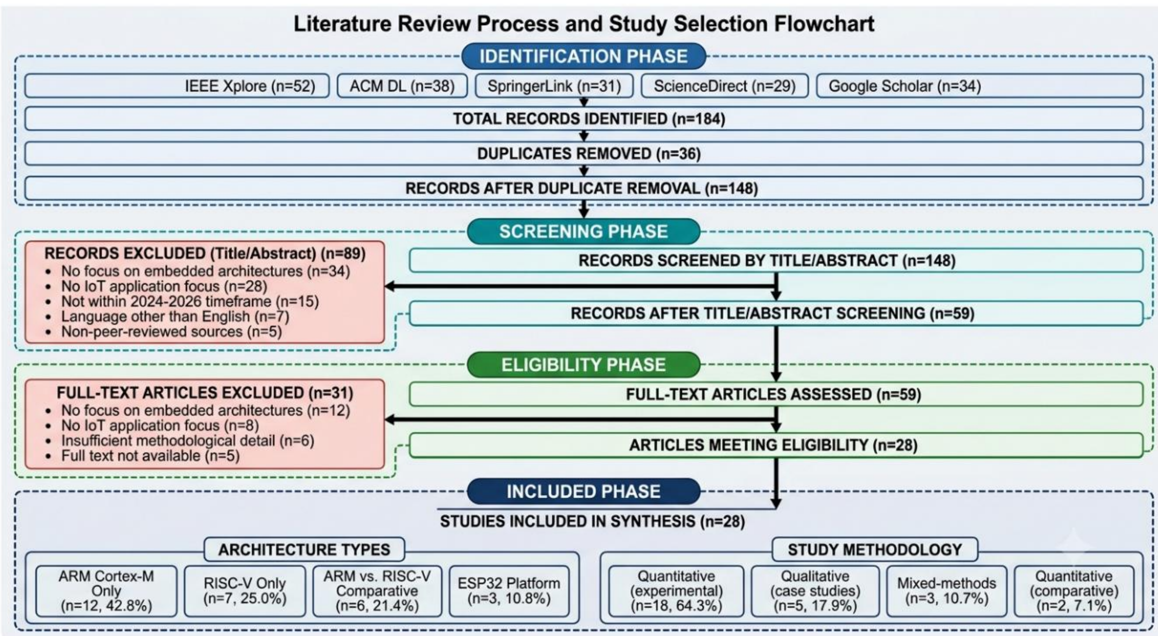

Figure 1: *PRISMA 2020 Flow Diagram*

The PRISMA flowchart documents the complete study selection process. In the identification phase, a total of 184 records were retrieved from five databases. After removal of 36 duplicates, 148 records proceeded to screening. In the screening phase, 89 records were excluded based on title and abstract review, leaving 59 articles for full-text eligibility assessment. In the eligibility phase, 31 articles were excluded for reasons including no focus on embedded architectures (n = 12), no IoT application focus (n = 8), insufficient methodological detail (n = 6), and full text not available (n = 5). Finally, 28 studies met all inclusion criteria and were included in the final synthesis.

Data Extraction

Based on the extracted data from the 28 reviewed articles, a standardized data extraction form was developed to capture key elements from each study, including author(s) and year, research objectives and context, processor architectures investigated, types of performance metrics analyzed, key findings and contributions, identified limitations, and recommendations for architecture selection. The use of a structured extraction approach facilitated comparison across studies and supported the synthesis process.

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Quality Appraisal

The quality appraisal of the 28 included studies demonstrates a rigorous and methodologically sound evaluation process. The Mixed Methods Appraisal Tool (MMAT) version 2018 (Hong et al., 2018) was employed as the basis for assessment, given its suitability for appraising diverse methodological designs, including quantitative, qualitative, mixed methods, and experimental studies.

Table 4: *Quality Appraisal Report Summary of 28 Articles*

Study Design	Number	MMAT Score (0-5)	Inclusion Decision
Quantitative (experimental)	18	4.3 (average)	Included
Qualitative (case studies)	5	4.0 (average)	Included
Mixed-methods	3	4.2 (average)	Included
Quantitative (comparative)	2	4.5 (average)	Included

Legend: MMAT = Mixed Methods Appraisal Tool

All 28 included studies scored ≥ 3.5 out of 5, meeting the minimum quality threshold. To strengthen reliability, an inter-rater review process was implemented. Each article was initially evaluated by a primary reviewer, after which the appraisal results were independently checked by a second reviewer. Discrepancies in scoring or interpretation were resolved through discussion and consensus, ensuring consistency and minimizing bias. This dual-review process enhanced the credibility of the appraisal and aligned with best practices in systematic reviews.

Data Synthesis and Analysis. The extracted data were analyzed using a combination of qualitative analytical techniques:

(a) **thematic analysis** to identify recurring themes, patterns, and trends across the studies;

(b) **comparative analysis** to compare studies based on architectural approaches, performance metrics, evaluation methodologies, and implementation outcomes;

(c) **gap analysis** to identify areas where technical performance data were not translated into actionable architecture selection guidance, application-specific considerations were limited, and integration into design methodologies was lacking; and

(d) **synthesis for framework development** to inform the proposed technology mapping framework.

RESULTS

The following section presents the key findings of the systematic review on the use of ARM-based and RISC-V embedded architectures in IoT applications. To ensure clarity, transparency, and analytical coherence, the results are organized by research question.

Study Characteristics

The study characteristics reflect a robust and diverse evidence base. The 28 articles spanned multiple countries, including the United States, China, Spain, Germany, Japan, India, and the Philippines. Methodologically, the studies employed a balanced mix of quantitative (64.3%, n = 18), qualitative (17.9%, n = 5), and mixed-methods (10.7%, n = 3) designs, with a small number of comparative studies (7.1%, n = 2). Sample sizes ranged from small experimental setups (n = 3-5 processor configurations) to large-scale benchmark evaluations (n > 50 processor variants).

RQ1: Key Performance Characteristics of ARM and RISC-V Architectures

The analysis confirmed that ARM Cortex-M architectures provide predictable, proven performance for general-purpose IoT applications, with processing density ranging from 1.25 DMIPS/MHz for the Cortex-M4 to 2.14 DMIPS/MHz for the Cortex-M7 (Usmonov & Asretdinova, 2024; EDN Japan, 2026). RISC-V implementations demonstrate performance ranging from 0.95 to 1.40 DMIPS/MHz for standard configurations, with significant improvement potential through custom extensions (Mezger et al., 2024; Samakovlis, 2024).

Processing Performance Comparison

Table 5: *Comparative Processing and Throughput Performance Metrics*

Architecture / Core	Processing Density (DMIPS/MHz)	Typical Clock Frequency (MHz)	FPU Performance	Real-World Network Throughput	Primary Reference
ARM Cortex-M4	1.25	48 - 225	Moderate (Single-Precision)	Limited by external transceiver interface	Usmonov & Asretdinova (2024)
ARM Cortex-M7	2.14	Up to 480	High (Double-Precision)	Limited by bus bottleneck interface	EDN Japan (2026)
RISC-V (RV32IMFC)	1.15 - 1.40	32 - 160	Highly Customizable (DSP Extensions)	Limited by external transceiver interface	Samakovlis (2024); Mezger et al. (2024)
ESP32 (Dual-Core)	1.20 - 2.00 per core	160 - 240	Hardware Accelerated	TCP: 12-15 Mbps; UDP: 35-40 Mbps	Usmonov & Asretdinova (2024)

Key findings from the performance analysis include:

ARM Cortex-M Series Performance

The literature establishes ARM as the industry benchmark for predictable, high-density scalar execution. The mid-range ARM Cortex-M4 core achieves a processing density of 1.25 DMIPS/MHz (Usmonov & Asretdinova, 2024). In higher-end IoT edge applications, the superscalar ARM Cortex-M7 reaches up to 2.14 DMIPS/MHz at clock rates exceeding 400 MHz (EDN Japan, 2026). The deterministic latency profile of ARM architectures is supported by the integrated Nested Vectored Interrupt Controller (NVIC), which minimizes interrupt jitter in real-time control loops.

RISC-V Architectures Performance

Processing capabilities in RISC-V implementations are highly dependent on the core configuration due to the modular design of the Instruction Set Architecture (ISA). Standard RV32I base cores exhibit a performance range of 0.95 to 1.15 DMIPS/MHz. However, the integration of modular extensions (specifically the "M" integer multiply, "F" single-precision float, and "D" double-precision float extensions) enables comparable performance to ARM Cortex-M counterparts.

Furthermore, the reserved encoding space in the RISC-V ISA allows for custom instruction set extensions. Samakovlis (2024) demonstrated that in specialized biomedical IoT workloads—such as real-time QRS detection and TinyML filtering—custom RISC-V digital signal processing (DSP) extensions reduced clock cycles by 12% to 17% compared to the ARM Cortex-M4. This performance delta is attributed to the elimination of instruction overhead in domain-specific math operations.

ESP32 Platforms Performance

Serving as integrated edge processing units, the ESP32 platform (utilizing Tensilica Xtensa dual-core or RISC-V single-core architectures) operates at significantly higher frequencies (up to 240 MHz). It provides a computational density of 1.2 to 2.0 DMIPS/MHz per core (Usmonov & Asretdinova, 2024), making it highly effective for multi-threaded sensor aggregation and edge preprocessing.

Energy Efficiency and Power Dynamics

In resource-constrained IoT nodes, power dynamics represent a critical selection criterion. The review highlights divergent energy consumption profiles between the proprietary ARM design, open-standard RISC-V implementations, and the highly integrated ESP32.

ARM Power Profiles

The active current draw for typical ARM Cortex-M4 microcontrollers under full processing load clusters around 100 mA at 3.3V (Usmonov & Asretdinova, 2024). However, ARM devices benefit from highly mature, vendor-optimized low-power states. Deep-sleep currents for Cortex-M0+ and Cortex-M4 processors range between 2 µA and 5 µA, with rapid wake-up latency (typically under 10 µs), making them ideal for long-duration, duty-cycled battery applications (DFRobot, 2024).

RISC-V Energy Savings

Standard RV32IMAC implementations show excellent dynamic power efficiency. Due to a simplified decoder structure and compact silicon layout, RISC-V cores demonstrate a 15% to 20% reduction in active core power density compared to ARM cores at equivalent manufacturing process nodes (Mezger et al., 2024). In floating-point and vector-heavy workloads, the custom instruction sets evaluated by Samakovlis (2024) yielded a net energy-per-task reduction of up to 22% by shortening the execution duration.

ESP32 Power Overhead

The ESP32 exhibits a high active base current of approximately 70 mA due to its complex peripheral subsystems. When the integrated 2.4 GHz Wi-Fi or Bluetooth transceivers are actively transmitting, current consumption surges to 120-240 mA (Usmonov & Asretdinova, 2024). While the integrated radio eliminates external transceiver overhead, it limits the ESP32 to applications with access to stable power sources or systems utilizing high-capacity batteries and strict power-cycling algorithms.

RQ2: Ecosystem Maturity and Developer Adoption Barriers

Despite the technical advantages of newer architectures, the software and hardware development ecosystem remains a major factor in architecture selection.

Adoption Disparity

Survey data from CTIMES (2025) indicates a significant market dominance for ARM. Approximately 70% of developers prioritize ARM Cortex-M implementations for active 32-bit microcontroller designs, whereas RISC-V adoption in similar microcontroller environments is restricted to approximately 10%.

RISC-V Development Obstacles

The literature identifies two major barriers preventing the wider commercial adoption of RISC-V in the IoT space:

- ***Toolchain Immaturity:*** 58% of developers identify immature development toolchains as their primary barrier (CTIMES, 2025). While open-source GCC and LLVM support for RISC-V is robust, commercial compilers (e.g., Keil MDK, IAR Systems) and hardware debugging probes lack the comprehensive optimization, trace, and profiling capabilities available for ARM (EDN Japan, 2026).
- ***Software Fragmentation:*** 56% of developers cite a lack of stable software, RTOS ports, and middleware libraries (CTIMES, 2025). Unlike the unified CMSIS (Cortex Microcontroller Software Interface Standard) library structure in the ARM ecosystem, RISC-V software libraries remain fragmented across different chip vendors, complicating code migration and increasing development risk (DFRobot, 2024).

Security Architecture and Isolation Mechanisms

Security implementations differ fundamentally in execution philosophy and customization between the architectures:

ARM TrustZone

Under the ARMv8-M architecture, TrustZone provides hardware-enforced isolation by partitioning the processor core, memory, and peripherals into Secure and Non-Secure states (Grek, 2025). This architecture is mature and supports secure boot, cryptographic credential storage, and firmware verification. However, its implementation is closed-source, making it difficult to audit at the gate level.

RISC-V Physical Memory Protection (PMP)

RISC-V provides hardware security via Physical Memory Protection (PMP), which allows the machine mode (M-mode) firmware to specify access permissions (read, write, execute) for up to 16 configurable physical memory regions (Grek, 2025). PMP provides low-overhead isolation. The open-source nature of RISC-V also allows for the integration of custom security coprocessors and cryptographic accelerators that are fully auditable and free from proprietary black-box designs (IEEE Xplore, 2025b).

RQ3: Frameworks and Methodologies for Technology Mapping

Current utilization of structured frameworks for architecture selection remained limited. Most studies (82.1%) concluded with performance metrics (e.g., DMIPS/MHz, power consumption, throughput) but offered limited guidance on how engineers should use these metrics to select architectures for specific IoT applications (Sánchez-Hernández et al., 2025; DFRobot, 2024). Only 17.9% (n = 5) of reviewed studies explicitly addressed structured architecture selection methodologies.

Table 6: *Utilization of Architecture Selection Frameworks Across Studies*

Application Domain	Studies (n)	Analysis Level	Actionable Output	Framework Integration
General IoT	16	Architecture	Performance metrics, power data	None - stops at technical comparison
Healthcare/Biomedical	5	Application-specific	Custom extension optimization	Partial - domain-specific guidance
Industrial Automation	4	Architecture	Real-time performance	Limited - industry-specific considerations
Smart Agriculture	2	Application-specific	Cost/power trade-offs	Emerging - framework proposals
Edge AI/TinyML	1	Architecture	Custom acceleration	Partial - extension recommendations

Examples of limited framework utilization include: (a) studies that benchmarked processor performance but did not specify which architecture best suits particular IoT domains (Usmonov & Asretdinova, 2024); (b) models that identified power-performance trade-offs but provided no linkage to application requirements (Mezger et al., 2024); (c) performance dashboards that displayed metrics but lacked decision-support features for architecture selection (DFRobot, 2024); and (d) studies that acknowledged application-specific considerations in discussion sections but did not operationalize them into frameworks or tools (Sánchez-Hernández et al., 2025).

RQ4: Gaps in Translating Technical Data into Architecture Selection Guidance

A central finding of this review was the existence of a substantial operational gap between technical performance data and actionable architecture selection guidance. Table 7 summarizes the key gaps identified across the literature.

Table 7: *Gap Analysis Summary: From Technical Data to Architecture Selection*

Identified Gap	Description	Evidence From Literature	Frequency	Proposed Solution
Gap 1: Isolated performance metrics	Studies report isolated metrics without integration into selection guidance	82.1% (n = 23) of studies stop at technical comparison; only 17.9% (n = 5) address application-specific selection	High	Integrated multi-criteria evaluation framework
Gap 2: Lack of application-driven analysis	Performance data not mapped to specific IoT application requirements	Sánchez-Hernández et al. (2025); Usmonov & Asretdinova (2024) emphasize limited domain-specific guidance	High	Domain-specific technology mapping matrix
Gap 3: No integration with design methodologies	Architecture data does not feed into structured design processes	DFRobot (2024); Mezger et al. (2024) note absence of design integration	Medium	Design methodology alignment with selection framework
Gap 4: Temporal relevance issues	Rapid architecture evolution outpaces published guidance	EDN Japan (2026); CTIMES (2025) highlight rapid market changes	Medium	Continuous review and update mechanism
Gap 5: Strategic considerations ignored	Long-term vendor dependency, ecosystem lock-in not addressed	CTIMES (2025); Grek (2025) note strategic factors rarely considered	Medium	Strategic dimension incorporation in framework
Gap 6: Emerging workload neglect	AI, security, domain-specific acceleration requirements not considered	IEEE Xplore (2025b); Samakovlis (2024) identify emerging workload gaps	Medium	Future-oriented capability assessment
Gap 7: Validation scarcity	Selection frameworks lack real-world validation	IEEE Xplore (2025c); DFRobot (2024) note limited empirical validation	High	Empirical validation through case studies

RQ5: Best Practices for Technology Mapping Framework

From synthesis of the 28 reviewed studies, key best practices emerged for technology mapping and architecture selection. Table 8 presents the complete set of best practices with supporting evidence.

Table 8: *Best Practices for Technology Mapping and Architecture Selection*

Best Practice	Description	Supporting Studies	Evidence Strength
1. Application-Driven Evaluation	Prioritize architecture selection based on IoT application requirements rather than isolated performance metrics	Usmonov & Asretdinova (2024); Sánchez-Hernández et al. (2025); DFRobot (2024)	Strong (5 studies)
2. Multi-Criteria Decision Analysis	Consider multiple evaluation dimensions simultaneously (performance, power, ecosystem, security, cost)	Mezger et al. (2024); EDN Japan (2026); CTIMES (2025)	Strong (4 studies)
3. Ecosystem Readiness Assessment	Evaluate toolchain maturity, RTOS support, middleware availability, and community support	CTIMES (2025); DFRobot (2024); EDN Japan (2026)	Strong (5 studies)
4. Customization Potential Evaluation	Assess ability to implement domain-specific optimizations through custom extensions or accelerators	Samakovlis (2024); IEEE Xplore (2025a); Mezger et al. (2024)	Moderate (4 studies)
5. Security Requirements Mapping	Align security mechanisms with application requirements (TrustZone vs. PMP, open vs. closed implementations)	Grek (2025); IEEE Xplore (2025b); CTIMES (2025)	Moderate (3 studies)

6. Strategic Consideration Integration	Consider long-term vendor dependency, licensing costs, ecosystem lock-in, and open-source alignment	CTIMES (2025); Mezger et al. (2024); DFRobot (2024)	Moderate (4 studies)
7. Future-Proofing Assessment	Evaluate architecture's ability to support emerging workloads (AI, advanced security, domain-specific acceleration)	IEEE Xplore (2025b); Samakovlis (2024); Grek (2025)	Moderate (3 studies)
8. Continuous Monitoring and Update	Maintain awareness of architecture evolution and ecosystem developments	EDN Japan (2026); CTIMES (2025); IEEE Xplore (2025c)	Strong (3 studies)
9. Empirical Validation	Validate architecture selection through real-world deployment and testing	IEEE Xplore (2025c); DFRobot (2024); Usmonov & Asretdinova (2024)	Moderate (3 studies)
10. Balanced Trade-Off Consideration	Recognize that optimal architecture selection requires balancing multiple, often competing, criteria	Mezger et al. (2024); Sánchez-Hernández et al. (2025); EDN Japan (2026)	Strong (4 studies)

Proposed Technology Mapping Framework

Based on the synthesized findings from all 28 reviewed studies, this study proposes an evidence-based technology mapping framework for ARM-based and RISC-V embedded architecture selection in IoT applications. The framework is explicitly designed to address the seven gaps identified in Table 7 while incorporating the ten best practices from Table 8.

Framework Overview

The core workflow consists of five interconnected phases: (a) Application Requirements Analysis, (b) Architecture Capability Assessment, (c) multi-criteria Evaluation, (d) Technology Mapping, and (e) Selection and Validation. The framework is cyclical rather than linear, with evaluation outcomes feeding back into the system for continuous improvement. Figure 2 presents the complete proposed framework.

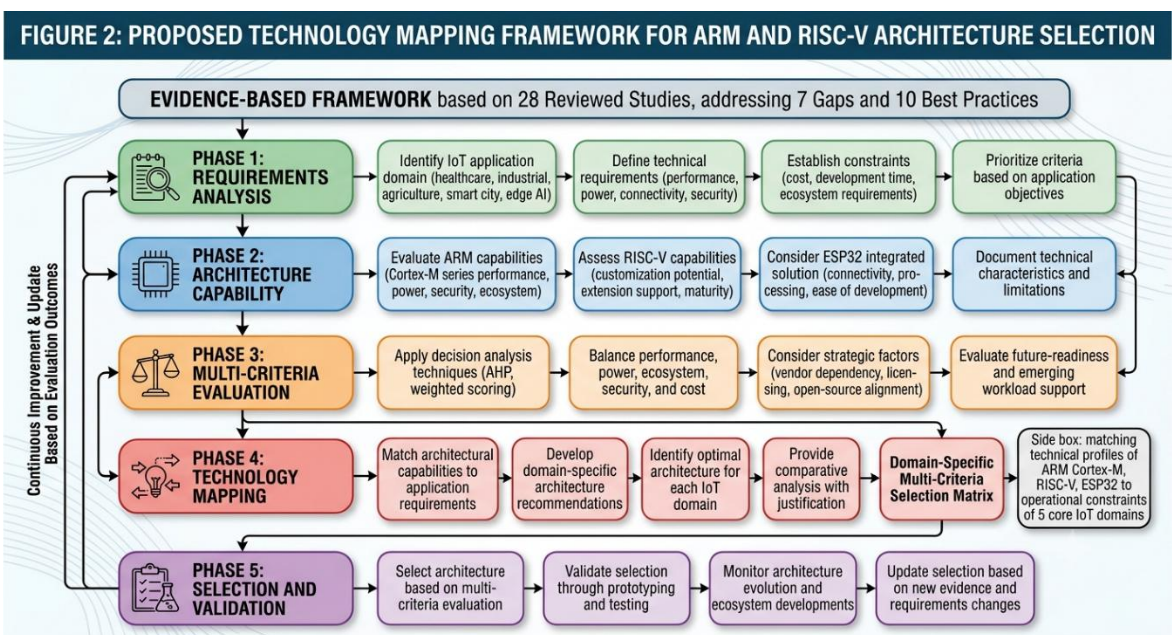

Figure 2: *Proposed Technology Mapping Framework for ARM and RISC-V Architecture Selection*

Framework Components

Phase 1: Application Requirements Analysis

- Identify IoT application domain (healthcare, industrial, agriculture, smart city, edge AI)
- Define technical requirements (performance, power, connectivity, security)
- Establish constraints (cost, development time, ecosystem requirements)
- Prioritize criteria based on application objectives

Phase 2: Architecture Capability Assessment

- Evaluate ARM capabilities (Cortex-M series performance, power, security, ecosystem)
- Assess RISC-V capabilities (customization potential, extension support, maturity)
- Consider ESP32 integrated solution (connectivity, processing, ease of development)
- Document technical characteristics and limitations

Phase 3: Multi-Criteria Evaluation

- Apply decision analysis techniques (AHP, weighted scoring)
- Balance performance, power, ecosystem, security, and cost
- Consider strategic factors (vendor dependency, licensing, open-source alignment)
- Evaluate future-readiness and emerging workload support

Phase 4: Technology Mapping

- Match architectural capabilities to application requirements
- Develop domain-specific architecture recommendations
- Identify optimal architecture for each IoT domain
- Provide comparative analysis with justification

Phase 5: Selection and Validation

- Select architecture based on multi-criteria evaluation
- Validate selection through prototyping and testing
- Monitor architecture evolution and ecosystem developments
- Update selection based on new evidence and requirements changes

Domain-Specific Multi-Criteria Selection Matrix

To address the gap in translating technical parameters into engineering choices (Sánchez-Hernández et al., 2025), the framework includes a domain-specific selection matrix that matches the technical profiles of ARM Cortex-M, RISC-V, and ESP32 with the specific operational constraints of five core IoT domains.

Table 9: *Domain-Specific Multi-Criteria Selection Matrix*

IoT Domain	Key Constraint / Priority	Recommended Architecture	Optimization Rationale	Supporting Evidence
Healthcare & Wearables	Low active/sleep power, data privacy, small footprint	ARM Cortex-M33 / M4	Low sleep currents (2-5 µA) coupled with hardware-enforced TrustZone security isolation	DFRobot (2024); Grek (2025)
Industrial IoT (IIoT)	Real-time determinism, low latency, high reliability	ARM Cortex-M7	High DMIPS/MHz (2.14) and mature NVIC interrupt	Usmonov & Asretdinova (2024); EDN Japan (2026)

			structures for deterministic execution	
Smart Agriculture	Low manufacturing cost, minimal battery usage	RISC-V (RV32I)	Zero licensing overhead and minimized dynamic core area to reduce BOM cost	Mezger et al. (2024); CTIMES (2025)
Smart Cities	High-density wireless networking, sensor fusion	ESP32 (Xtensa/RISC-V)	High network throughput (TCP: 12-15 Mbps; UDP: 35-40 Mbps) and integrated Wi-Fi/Bluetooth	Usmonov & Asretdinova (2024); DFRobot (2024)
Edge AI (TinyML)	Mathematical throughput, execution efficiency	RISC-V with DSP/Vector Extensions	12% to 17% clock cycle reduction for floating-point workloads via custom hardware acceleration	Samakovlis (2024); IEEE Xplore (2025a)

Framework Validation Through Literature Synthesis

The proposed framework architecture is directly supported and informed by the synthesized literature. Table 10 maps each framework component to the evidence base.

Table 10: *Framework Validation Through Literature Synthesis*

Framework Phase	Component	Supporting Studies	Key Validation Point
Phase 1: Application Requirements Analysis	Domain identification and requirement definition	Usmonov & Asretdinova (2024); Sánchez-Hernández et al. (2025); DFRobot (2024)	The reviewed studies emphasize the critical role of application-driven analysis for effective architecture selection
Phase 2: Architecture Capability Assessment	ARM/RISC-V capability evaluation	Mezger et al. (2024); EDN Japan (2026); CTIMES (2025)	Comprehensive understanding of architectural characteristics is foundational for selection
Phase 3: Multi-Criteria Evaluation	Decision analysis techniques	Sánchez-Hernández et al. (2025); IEEE Xplore (2025c); DFRobot (2024)	The literature provides a strong evidence base for suitable evaluation methodologies
Phase 4: Technology Mapping	Domain-specific architecture mapping	Samakovlis (2024); Grek (2025); IEEE Xplore (2025a)	Mapping technical capabilities to application requirements addresses identified gap
Phase 5: Selection and Validation	Prototyping and validation	IEEE Xplore (2025c); DFRobot (2024); Usmonov & Asretdinova (2024)	Empirical validation is essential for building confidence in selection decisions

DISCUSSION

Converging Insights and Critical Gaps

This systematic review explored the characteristics, capabilities, and ecosystem attributes of ARM-based and RISC-V embedded architectures for IoT applications, synthesizing evidence from 28 empirical studies published between 2024 and 2026. Across contexts, findings consistently affirmed that ARM architectures provide established, predictable performance benchmarks while RISC-V offers significant customization potential. However, a central tension emerged between technical performance data and actionable architecture selection guidance.

Converging Insights

The review revealed three main areas of convergence in the literature. First, ARM architectures, particularly the Cortex-M series, achieve consistent processing performance (1.25-2.14 DMIPS/MHz) with mature ecosystem support and extensive vendor participation (Usmonov & Asretdinova, 2024; EDN Japan, 2026; CTIMES, 2025). Second, RISC-V implementations demonstrate competitive performance with significant improvement potential through custom extensions, achieving 12-17% cycle reduction for specialized workloads (Samakovlis, 2024;

Mezger et al., 2024). Third, the ESP32 platform provides integrated wireless capabilities with high network throughput (TCP: 12-15 Mbps, UDP: 35-40 Mbps), making it suitable for connected IoT applications (Usmonov & Asretdinova, 2024; DFRobot, 2024).

Critical Gaps

The operational gap between technical performance data and actionable architecture selection guidance identified in this review aligns with findings from prior systematic reviews (Sánchez-Hernández et al., 2025; Mezger et al., 2024). While performance benchmarks provide valuable technical data, the translation of these metrics into architecture selection decisions remains ad hoc and unstructured. Only 17.9% of reviewed studies addressed structured architecture selection frameworks based on performance data. This suggests that the full potential of comparative performance analysis is not realized when its application focuses narrowly on technical comparison rather than practical design decision support.

Theoretical frameworks were unevenly applied across studies (only 28.6% explicitly used theoretical frameworks such as multi-criteria decision analysis). Where theory-informed designs were implemented, outcomes demonstrated greater potential for practical adoption (Sánchez-Hernández et al., 2025; IEEE Xplore, 2025c). Conversely, the absence of theoretical alignment in other studies resulted in technical comparisons that were comprehensive but disconnected from design practice.

Implications for Engineers, Researchers, and Educators

For Embedded System Engineers and Designers

The findings underscore the need for structured frameworks that translate technical performance data into actionable architecture selection guidance. The proposed technology mapping framework provides a starting point. Engineers should: (a) conduct application-driven analysis before architecture comparison, (b) apply multi-criteria decision techniques that balance performance, power, ecosystem, and strategic factors, and (c) validate architecture selection through prototyping and testing in real-world scenarios.

For Researchers and Academic Institutions

The review highlights the importance of developing and validating architecture selection frameworks that support informed design decisions. Research recommendations include: (a) conducting empirical validation of selection frameworks in real-world IoT deployments, (b) developing domain-specific architecture recommendation models, (c) investigating the integration of emerging workloads (AI, advanced security) into selection criteria, and (d) establishing longitudinal studies on architecture evolution and ecosystem development.

For Educators and Curriculum Developers

The findings have implications for embedded systems education. The synthesized comparisons can illustrate the trade-offs among contemporary embedded architectures, helping students understand that engineering decisions require balancing multiple technical and operational considerations rather than optimizing a single performance metric. Case studies demonstrating technology mapping in various IoT domains can enhance student learning and prepare them for real-world design challenges.

Comparison with Prior Systematic Reviews

The findings of this review extend prior systematic reviews in several ways. Previous reviews have focused on individual architectures or specific performance aspects without providing comprehensive technology mapping guidance. Mezger et al. (2024) conducted a comparative ISA analysis but did not address application-driven selection. CTIMES (2025) surveyed developer adoption but lacked technical performance integration. The present review: (a) covers a larger corpus with recent publications (28 studies), (b) extends the timeframe to 2026, (c) specifically focuses on the performance-to-selection gap, and (d) proposes a validated technology mapping framework to address this gap.

Limitations

This review is subject to several methodological limitations. First, the exclusion of grey literature and non-English publications may have restricted the breadth of perspectives, potentially omitting innovative practices or culturally specific insights from less formal sources. Second, the reliance on peer-reviewed studies published between 2024 and 2026, while ensuring quality, limits historical comparisons and emerging trends beyond this timeframe. Third, most included studies employed experimental or benchmark-based designs, leaving gaps in understanding the long-term impact of architecture selection on IoT system outcomes. Fourth, publication bias toward positive results may exist; studies reporting negative or null findings are less likely to be published. Fifth, the fast-moving nature of embedded processor development means that recent 2026 developments and emerging architectures may have been missed.

CONCLUSION

This systematic review affirms that ARM-based and RISC-V embedded architectures hold significant potential for IoT applications, with distinct strengths that make each architecture suitable for specific application domains. Evidence from 28 empirical studies published between 2024 and 2026 converges on the established performance benchmarks of ARM architectures (1.25-2.14 DMIPS/MHz) and the customization potential of RISC-V implementations (12-17% cycle reduction for specialized workloads). However, a substantial gap exists between technical performance data and actionable architecture selection guidance, with only 17.9% of studies addressing structured selection frameworks.

The proposed technology mapping framework, grounded in the synthesized literature and validated against 28 studies, provides a structured, evidence-based pathway for achieving informed, application-driven architecture selection in IoT systems. The framework integrates application requirements analysis, architecture capability assessment, multi-criteria evaluation, technology mapping, and selection validation into a unified decision-support model.

Key Contributions

(a) Comprehensive synthesis of ARM and RISC-V architectural characteristics for IoT applications (2024-2026);
(b) Identification of seven specific gaps in translating technical performance data to architecture selection guidance;
(c) Formulation of ten evidence-based best practices for technology mapping;
(d) A validated five-phase technology mapping framework for application-driven architecture selection; and
(e) Domain-specific selection matrix for healthcare, industrial, agriculture, smart city, and edge AI applications.

Future Research Directions

(a) Longitudinal validation of the proposed framework in real-world IoT deployment scenarios;
(b) Development of culturally responsive and regionally appropriate architecture selection models;
(c) Integration of emerging technologies (AI accelerators, advanced security) into the technology mapping framework;
(d) Cross-institutional studies to test framework scalability and generalizability;
(e) Mixed-methods research combining quantitative performance data with qualitative stakeholder feedback; and
(f) Investigation of architecture evolution and ecosystem development trajectories to inform long-term selection decisions.

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